a display; and

a processor, wherein said processor transfers data stored in each of said addresses of said main memory area to said spare memory area upon a number of write operations performed to a respective one of said addresses in said main memory reaching a predetermined value, and wherein said processor drives said display to display a remaining amount of said storage capacity in said spare memory upon a remaining amount of said storage capacity reaching a predetermined remaining capacity.

14. The memory unit as in claim 13, wherein said processor compares said remaining amount of said storage capacity with a plurality of different values of said predetermined remaining capacity, wherein the comparison produces a plurality of different results, and wherein said processor drives said display in different manners dependent upon said plurality of different results.

15. The memory unit as in claim 13, wherein said processor drives the display upon said number of write operations performed to a respective one of said addresses in said main memory reaching a predetermined number.

16. A memory unit comprising:

a memory having a main memory area and a spare memory area, wherein said main memory area includes a plurality of data storage registers and wherein each of said

data storage registers has an address, and wherein said spare memory area has a storage capacity;

a display; and

a processor, wherein said processor transfers data stored in each of said addresses of said main memory area to said spare memory area upon an error frequency within one of said plurality of data storage registers reaching a predetermined frequency, and wherein said processor drives said display to display a remaining amount of said storage capacity in said spare memory upon a remaining amount of said storage capacity reaching a predetermined remaining capacity.

17. The memory unit of claim 16, wherein said processor compares said remaining amount of said storage capacity with a plurality of different values of said predetermined remaining capacity, wherein the comparison produces a plurality of different results, and wherein said processor drives said display in different manners dependent upon said plurality of different results.

18. The memory unit of claim 16, wherein said processor drives the display upon said error frequency reaching a predetermined frequency.

19. A memory unit comprising a main memory area and a spare memory are, wherein said main memory area includes a plurality of data storage registers and wherein each of data storage registers has an address, and wherein said spare memory area has a storage capacity;

a display; and

a processor, wherein said processor transfers data stored under each of said addresses of said main memory area to said spare memory area upon a number of write operations performed to a respective one of said addresses in said main memory reaching a predetermined value, and wherein said processor outputs a signal to an external unit upon a remaining amount of said storage capacity reaching a predetermined remaining capacity, and wherein said signal is representative of said remaining amount of said storage capacity.

20. The memory unit of claim 19, wherein said processor compares said remaining amount of said storage capacity with a plurality of different values of said predetermined remaining capacity, wherein each of the comparisons produces a result, and wherein said processor outputs said result to said external unit.

21. The memory unit of claim 19, wherein said processor outputs said signal to said external unit upon said number of write operations performed to a respective one of said addresses in said main memory reaching a predetermined number.

22. A memory unit comprising:

a memory having a main memory area and a spare memory area, wherein said main memory area includes a plurality of data storage registers and wherein each of said